Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 9, 15, 24, 40 and 42-54, amend claims 1, 13, 16-21, 23, 25-27 and 32, and add new claims 55-109 as follows:

Listing of Claims:

1. (Currently Amended) A semiconductor structure comprising:

a substrate material and a composite laminate dielectric layer formed on the substrate material, the composite laminate dielectric layer comprising;

a layer of ZrO_2; and

a layer of a lanthanide oxide having a thickness of about 2 –12 nm on the ZrO_2 layer.

2. (Original) The semiconductor structure of claim 1 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

3. (Original) The semiconductor structure of claim 1 wherein the composite laminate dielectric layer is a gate dielectric layer of a transistor.

4. (Original) The semiconductor structure of claim 3 wherein the transistor is a component of a DRAM.

5. (Original) The semiconductor structure of claim 1 wherein the composite laminate dielectric layer is a dielectric layer of a capacitor.

6. (Original) The semiconductor structure of claim 5 wherein the capacitor is a component of a DRAM.

7. (Original) The semiconductor structure of claim 1 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

8. (Original) The semiconductor structure of claim 1 wherein the ZrO_2 layer has a thickness of about 1–6 nm.

9. (Canceled)

10. (Original) The semiconductor structure of claim 1 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.

11. (Original) The semiconductor device of claim 1 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

12. (Original) The semiconductor device of claim 1 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

13. (Currently Amended) A semiconductor transistor comprising:

a gate electrode;

a source region and a drain region; and

a gate dielectric layer beneath the gate electrode and between the source and the drain regions, the dielectric layer being a composite laminate dielectric layer having a thickness of about 2–5 nm comprising a first layer of ZrO_2 , and a second layer of lanthanide oxide.

14. (Original) The semiconductor transistor of claim 13 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

15. (Canceled)

16. (Currently Amended) The semiconductor ~~structure~~ transistor of claim 13 wherein the lanthanide oxide layer has a thickness of about 2 –12 nm.

17. (Currently Amended) The semiconductor ~~structure~~ transistor of claim 13 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.

18. (Currently Amended) The semiconductor ~~structure~~ transistor of claim ~~1~~ 13 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

19. (Currently Amended) The semiconductor ~~structure~~ transistor of claim ~~1~~ 13 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

20. (Currently Amended) The semiconductor ~~structure~~ transistor of claim 13 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

21. (Currently Amended) +24 A semiconductor capacitor comprising:

a first electrode;

a second electrode, and

a dielectric layer separating the first and the second electrodes, the dielectric layer being a composite laminate dielectric layer comprising a first layer of ZrO_2 having a thickness of about 1-2 nm, and a second layer of lanthanide oxide.

22. (Original) The semiconductor capacitor of claim 21 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

23. (Currently Amended) The semiconductor ~~structure~~ capacitor of claim 21 wherein the ZrO_2 layer has a thickness of about 1-6 nm.

24. (Canceled)

25. (Currently Amended) The semiconductor ~~structure~~ capacitor of claim 21 wherein the ZrO_2 layer has a thickness of about 3 nm.

26. (Currently Amended) The semiconductor capacitor of claim 21 wherein the lanthanide oxide layer has a thickness of about 2-4 nm.

27. (Currently Amended) The semiconductor capacitor of claim 21 wherein the lanthanide oxide layer has a thickness of about 3 nm.

28. (Original) The semiconductor capacitor of claim 21 wherein the composite laminate dielectric layer has a thickness of about 9 nm.

29. (Original) The semiconductor capacitor of claim 21 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

30. (Original) The semiconductor capacitor of claim 21 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

31. (Original) The semiconductor capacitor of claim 21 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

32 (Original) A semiconductor memory device comprising:

a capacitor that includes a first dielectric material separating a first and a second electrode;

a transistor that includes a second dielectric material beneath a gate electrode and between a source and a drain region, and

at least one of the first and second dielectric materials is a composite laminate dielectric layer comprised of a first layer of material selected from the group consisting of ZrO_2 and lanthanide oxide and a second layer of material selected from the group consisting of ZrO_2 and a lanthanide oxide on the first layer of material, the second layer of material being different from the first layer of material, wherein if the first or second layer is lanthanide oxide, the lanthanide oxide layer has a thickness of about 2 –12 nm.

33. (Original) The semiconductor memory device of claim 32 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

34. (Original) The semiconductor memory device of claim 32 wherein the first dielectric material is comprised of the composite laminate dielectric layer.

35. (Original) The semiconductor memory device of claim 32 wherein the second dielectric material is comprised of the composite laminate dielectric layer.

36. (Original) The semiconductor memory device of claim 32 wherein the wherein each of the first and the second dielectric material is comprised of the composite laminate dielectric layer.

37. (Original) The semiconductor memory device of claim 32 wherein the device is a DRAM.

38. (Original) The semiconductor memory device of claim 32 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

39. (Original) The semiconductor memory device of claim 32 wherein the ZrO_2 layer has a thickness of about 1–6 nm.

40. (Canceled)

41. (Original) The semiconductor memory device of claim 32 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.

42-54 (Canceled)

55. (New) A semiconductor structure comprising:

a substrate material and a composite laminate dielectric layer having a thickness of about 3-18 nm formed on the substrate material, the composite laminate dielectric layer comprising;

a layer of ZrO_2; and

a layer of a lanthanide oxide on the ZrO_2 layer.

56. (New) The semiconductor structure of claim 55 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

57. (New) The semiconductor structure of claim 55 wherein the composite laminate dielectric layer is a gate dielectric layer of a transistor.

58. (New) The semiconductor structure of claim 57 wherein the transistor is a component of a DRAM.

59. (New) The semiconductor structure of claim 55 wherein the composite laminate dielectric layer is a dielectric layer of a capacitor.

60. (New) The semiconductor structure of claim 59 wherein the capacitor is a component of a DRAM.

61. (New) The semiconductor structure of claim 55 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

62. (New) The semiconductor structure of claim 55 wherein the ZrO_2 layer has a thickness of about 1–6 nm.

63. (New) The semiconductor structure of claim 55 wherein the lanthanide oxide layer has a thickness of about 2 –12 nm.

64. (New) The semiconductor device of claim 55 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

65. (New) The semiconductor device of claim 55 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

66. (New) A semiconductor transistor comprising:

a gate electrode;

a source region and a drain region; and

a gate dielectric layer beneath the gate electrode and between the source and the drain regions, the dielectric layer being a composite laminate dielectric layer comprising a first layer of ZrO_2 and a second layer of lanthanide oxide having a thickness of about 2 –12 nm.

67. (New) The semiconductor transistor of claim 66 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

68. (New) The semiconductor transistor of claim 66 wherein the ZrO_2 layer has a thickness of about 2–5 nm.

69. (New) The semiconductor transistor of claim 66 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.

70. (New) The semiconductor transistor of claim 66 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

71. (New) The semiconductor transistor of claim 66 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

72. (New) The semiconductor transistor of claim 66 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

73. (New) A semiconductor transistor comprising:

a gate electrode;

a source region and a drain region; and

a gate dielectric layer beneath the gate electrode and between the source and the drain regions, the dielectric layer being a composite laminate dielectric layer having a thickness of about 3-18 nm comprising a first layer of ZrO_2 and a second layer of lanthanide oxide.

74. (New) The semiconductor transistor of claim 73 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

75. (New) The semiconductor transistor of claim 73 wherein the ZrO_2 layer has a thickness of about 2–5 nm.

76. (New) The semiconductor transistor of claim 73 wherein the lanthanide oxide layer has a thickness of about 2 –12 nm.

77. (New) The semiconductor transistor of claim 73 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

78. (New) The semiconductor transistor of claim 73 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

79. (New) The semiconductor transistor of claim 73 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

80. (New) A semiconductor capacitor comprising:

a first electrode;

a second electrode, and

a dielectric layer separating the first and the second electrodes, the dielectric layer being a composite laminate dielectric layer comprising a first layer of ZrO_2 and a second layer of lanthanide oxide having a thickness of about 2-4 nm.

81. (New) The semiconductor capacitor of claim 80 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

82. (New) The semiconductor capacitor of claim 80 wherein the ZrO_2 layer has a thickness of about 1-6 nm.

83. (New) The semiconductor capacitor of claim 80 wherein the ZrO_2 layer has a thickness of about 1-2 nm.

84. (New) The semiconductor capacitor of claim 80 wherein the ZrO_2 layer has a thickness of about 3 nm.

85. (New) The semiconductor capacitor of claim 80 wherein the lanthanide oxide layer has a thickness of about 3 nm.

86. (New) The semiconductor capacitor of claim 80 wherein the composite laminate dielectric layer has a thickness of about 9 nm.

87. (New) The semiconductor capacitor of claim 80 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

88. (New) The semiconductor capacitor of claim 80 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

89. (New) The semiconductor capacitor of claim 80 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

90. (New) A semiconductor capacitor comprising:

a first electrode;

a second electrode, and

a dielectric layer separating the first and the second electrodes, the dielectric layer being a composite laminate dielectric layer having a thickness of about 9 nm comprising a first layer of ZrO_2 and a second layer of lanthanide oxide.

91. (New) The semiconductor capacitor of claim 90 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

92. (New) The semiconductor capacitor of claim 90 wherein the ZrO_2 layer has a thickness of about 1-6 nm.

93. (New) The semiconductor capacitor of claim 90 wherein the ZrO_2 layer has a thickness of about 1-2 nm.

94. (New) The semiconductor capacitor of claim 90 wherein the ZrO_2 layer has a thickness of about 3 nm.

95. (New) The semiconductor capacitor of claim 90 wherein the lanthanide oxide layer has a thickness of about 2-4 nm.

96. (New) The semiconductor capacitor of claim 90 wherein the lanthanide oxide layer has a thickness of about 3 nm.

97. (New) The semiconductor capacitor of claim 90 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

98. (New) The semiconductor capacitor of claim 90 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

99. (New) The semiconductor capacitor of claim 90 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

100 (New) A semiconductor memory device comprising:

a capacitor that includes a first dielectric material separating a first and a second electrode;

a transistor that includes a second dielectric material beneath a gate electrode and between a source and a drain region, and

at least one of the first and second dielectric materials is a composite laminate dielectric layer having a thickness of about 3-18 nm comprised of a first layer of material selected from the group consisting of ZrO_2 and lanthanide oxide and a second layer of material selected from the group consisting of ZrO_2 and a lanthanide oxide on the first layer of material, the second layer of material being different from the first layer of material.

101. (New) The semiconductor memory device of claim 32 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

102. (New) The semiconductor memory device of claim 32 wherein the first dielectric material is comprised of the composite laminate dielectric layer.

103. (New) The semiconductor memory device of claim 32 wherein the second dielectric material is comprised of the composite laminate dielectric layer.

104. (New) The semiconductor memory device of claim 32 wherein the wherein each of the first and the second dielectric material is comprised of the composite laminate dielectric layer.

105. (New) The semiconductor memory device of claim 32 wherein the device is a DRAM.

106. (New) The semiconductor memory device of claim 32 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

107. (New) The semiconductor memory device of claim 32 wherein the ZrO_2 layer has a thickness of about 1–6 nm.

108. (New) The semiconductor memory device of claim 32 wherein the lanthanide oxide layer has a thickness of about 2 –12 nm.

109. (New) The semiconductor memory device of claim 32 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.